

## REMARKS

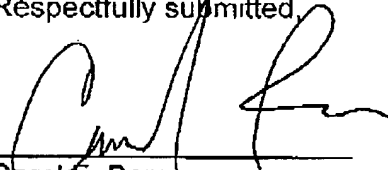
MAR 12 2007

Claims 1-12 are pending. Claims 13-20 are withdrawn. Claims 1-4 are rejected under 35 U.S.C. § 102(b) based upon us Patent No. 5,914,522 issued to Aiello et al. Aiello is directed to VIPower technology. The device is made from a chip of N-type semiconductor material comprising a bipolar or field-effect vertical power transistor. The power transistor has a collector or drain region in the N-type material. The semiconductor structure comprises a PNP bipolar lateral power transistor having a base region in the N-type material in common with the collector or drain region of the vertical power transistor.

Claim 1 is directed to an implantable medical device that includes "a semiconductor substrate; an epitaxial layer overlying the semiconductor substrate; a power transistor formed in the epitaxial layer having a first electrode, a control electrode, and a second electrode wherein a breakdown voltage of the power transistor is greater than 100 volts and wherein current flow of the transistor is vertical through the epitaxial layer to the semiconductor substrate; a backside contact coupling to the first electrode of the power transistor, at least one deep trench etched through the epitaxial layer exposing the semiconductor substrate wherein the at least one deep trench is etched in an area outside the high voltage termination region; and a first electrode contact region coupling to the semiconductor substrate exposed by the at least one deep trench, the first electrode contact region overlying the epitaxial layer. The United States Patent & Trademark Office (USPTO) admitted that Aiello does not disclose teach or suggest the limitation from claim 5, which was included in amended claim 1. Instead, the USPTO asserts that US Patent Publication No. 20030213605 by Brendel et al. teaches this element. Applicants created their invention before Brendel. Support for Applicants assertion is found in the attached affidavits, invention disclosure statement, and notes. Applicants also assert that the USPTO has not met its burden of establishing a motivation to combine references. In particular, Applicants assert that the USPTO used Applicants claims as a blue print and then merely used a limitation-by-limitation reference-by reference analysis to establish its obviousness rejection. The

Federal Circuit has rejected such analysis. Withdrawal of the instant rejections and issuance of a Notice of Allowance is respectfully requested.

Respectfully submitted,



March 12, 2007  
Date

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**Medtronic****INVENTION DISCLOSURE FORM**

**WARNING:** Due to the confidential nature of this document, save it as a password protected document. Do not send this document through GroupWise.

This is a **WORD Template** form. Press **enter** or **tab** to move to each field. Please fill out this form as completely as possible. If the allotted space is not sufficient, use a separate sheet. Have your manager sign the form and forward it to the Patent Section of the Law Department, MS301. Please attach any drawings and technical descriptions that are available and assemble copies of the background articles, books, advertisements, etc. for use by your patent attorney.

1.
 

Inventor(s) Full Name(s)	Employee Number	Mail Stop	Home Address (Include Zip Code)
Mark Boone	22969	SS76-10	518 W. San Remo St., Gilbert, AZ 85233
Ralph Danzl	23269	SS76-22	1601E Westwind Way, Tempe, AZ 85283
Paul Gerrish	22224	SS76-10	14838 S. 30 <sup>th</sup> St., Phoenix, AZ 85048
Mike Mattes	61277	SS76-10	2173 E. Kempton Rd., Chandler, AZ 85225
Tyler Mueller	24051	SS76-10	4847 E. Francisco Dr. #246, Phoenix, AZ 85044
Jeff Van Wagoner	33831	SS76-22	2677 E. Libra St. Gilbert, AZ 85234
2. Title of Invention: Bumpable 1KV DMOS Device
3. Summary of the Invention: 1000V vertical mosfet, which is bumped, having a drain contact on the front surface of the die. Drain contact is made via a trench through the epi region down into the substrate. The mosfet obtains a low Rdson by having a high cell packing density, thus creating a multitude of current paths in parallel.
4. How have others addressed this problem (List and attach any patents, books, articles, devices, Medtronic or competitor's products, or other background materials you used or which may be prior art)? wire bond or other chip carriers
5. The invention is described on pages \_\_\_\_\_ of Lab Notebook No. \_\_\_\_\_ (Please attach copy).  
See Medtronic Microelectronics Center Specification 3212963.
6. When was a device built which included the invention? Development is underway.  
Who built it? Medtronic Microelectronics Center Where is it? 2343 W. 10<sup>th</sup> Place, Tempe, AZ 85281  
Who has supporting documents? SST Organization has design rule flow and Wafer Fab has a Promis Process Flow  
Who witnessed tests? \_\_\_\_\_ When and where? \_\_\_\_\_
7. Discuss the problems which the invention is designed to solve, referring to any prior devices of a similar nature with which you may be familiar. The invention provides a 1KV DMOS device which can be solder reflow attached to a circuit board. This invention eliminates the need for wirebondable devices.
8. State the advantages of the Invention over presently known devices, systems or processes. The invention provides a bumped, surface mountable 1KV DMOS device.
9. List all known and other possible uses for the invention. Other applicable high voltage device technologies
10. Specifically describe the invention and its operation. You may use and attach copies of sketches, prints, photographs and illustrations which should be signed, witnessed and dated. Use numbers and descriptive names in descriptions and drawings. See attached description and drawings
11. List all features of the invention that are believed to be novel. Etches in the <100> surface orientation to create a "trench" in the epitaxial silicon, allowing contact to the substrate-drain of the device (see Figure 1). A bumped 1KV DMOS vertical mosfet.
12. Sale or Publication (Needed to establish the date of any printed publication, public use or sale, since no U. S. patent application may be filed after one year from such date.)

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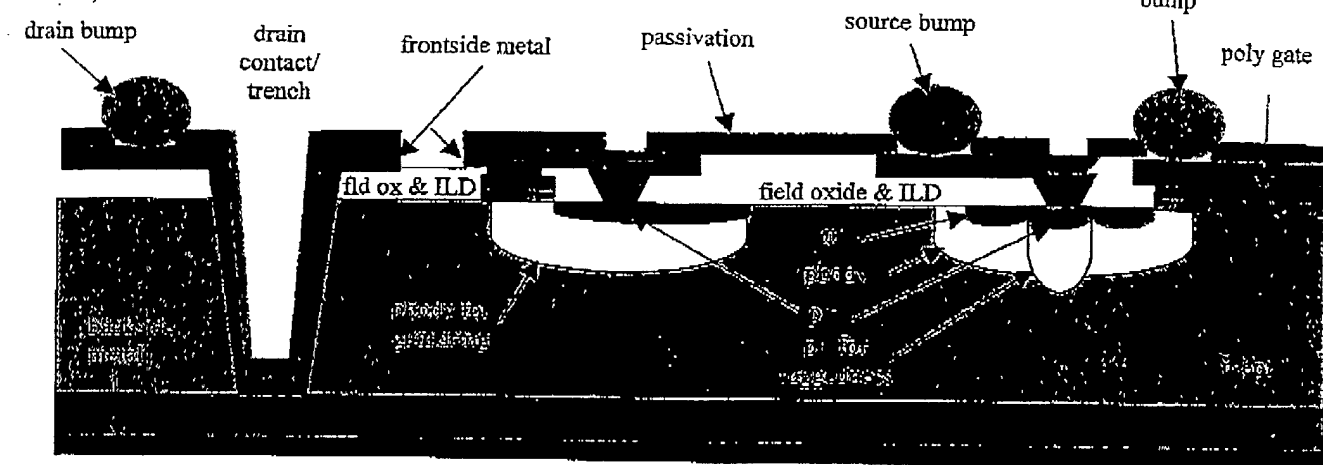
**Bumpable 1KV DMOS Device**

Figure 1 – Bumpable 1KV DMOS Device Simplified Cross Section

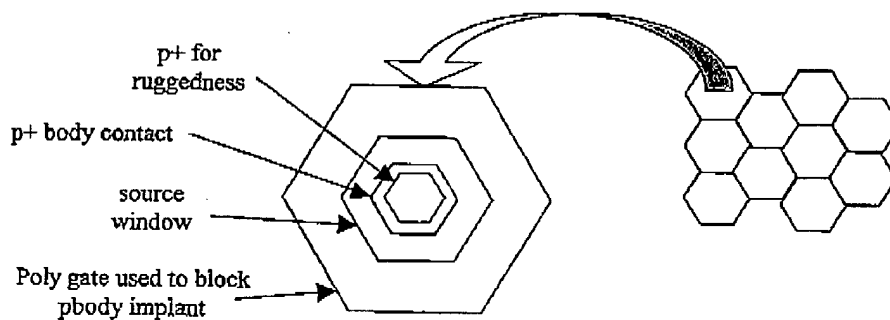


Figure 2 – Packing Density of the Hexagonal MOSFET Cell Construction with Expanded View of Layout Cell

**DEVICE CLAIMS (General)**

1. Trench etched in the  $\langle 100 \rangle$  crystal orientation; Allows drain-substrate contact.
2. Centered Gate Bump allows a more consistent gate voltage across the die.
3. Metal on backside of wafer reduces  $R_{ds(on)}$  of DMOS device.
4. Plurality of cells to maximize packing density of DMOS cells by using hexagonal cell construction.
5. Allows for smaller hybrid packaging area by eliminating the need for wire bonds and the space surrounding the die.
6. Field plates in the guardrings contact both metal and poly to alter the surface field potential.
7. Uses the patterned polysilicon as a blocking mask for the pbody implant.
8. For use in implantable medical devices.

Taken together we believe that the above claims, or subset, may be patentable.

**DEVICE CLAIMS (Specific)**

1. Device having a pbody diffusion junction depth between 6-9 $\mu$ m.
2. Device having a p+ junction extending slightly farther than the pbody diffusion for improved avalanche/ruggedness.
3. Device having a p+ source/drain implant overlapping the n+ source region for use as a body contact.
4. Device having a poly gate width between 19-22 $\mu$ m.
5. Device having a mosfet cell pitch between 30-40 $\mu$ m.
6. Device having a threshold voltage between 2 and 4 volts.
7. Device having an on state resistance ( $R_{ds(on)}$ ) of less than approximately 0.8 micro-ohms/ $\mu$ m<sup>2</sup>.
8. Device having the ability to hold off a minimum of 1000 volts drain to source.

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- a. If a device has been offered, or will be offered for sale, or used for profit or otherwise publicly disclosed, state when and to whom delivered and how used? n/a
- b. Has a printed description of this invention been made available to persons outside the company? How and when and was use restricted (e.g. licensing agreement, non-disclosure agreement, proprietary legends, etc.)?

Non-Disclosure Agreement

- Provided METAL and PAD data to facilitate manufacture of the bump stencil.
- Test wafer(s) were sent to facilitate verification of the bump stencil.
- Discussed bumping near the drain contact/trench.

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Colorado Springs, Colorado, USA 80907  
Phone: 719-533-1030  
Fax: 719-533-1021  
Email: [ici@icinterconnect.com](mailto:ici@icinterconnect.com)

## 13. Inventor(s) Signature(s) (REQUIRED):

Signature

[Signature]  
[Signature]  
[Signature]  
[Signature]  
[Signature]

Date

[Signature]  
[Signature]  
[Signature]  
[Signature]

## Manager's Comments

## 14. How is this invention important to your products, plans or goals?

FLIP CHIP HIGH POWER COMPONENTS ARE AN IMPORTANT  
FEATURE FOR SIMPLIFYING THE HYBRID ASSEMBLY PROCESS.  
HAVING ALL DIE BE SURFACE MOUNT FOR BOTH LOW VOLTAGE  
AND HIGH VOLTAGE ON ONE HYBRID IS DESIRABLE.

## 15. Manager's Signature (REQUIRED)

Signature

[Signature]  
Manager's Printed Name PAUL F. GEARISHT  
Business Unit CRM/IMC

Date

Mail Stop 10-6

Manager: Please forward to Patent Section of Law Department, MS 301, upon completion of your review.

\$GDPDC DCOP Z003G.04  
Entry constraint: DONTCARE/DONTCARE/DONTCARE/DONTCARE  
Exit constraint: NOCHANGE/NOCHANGE/NOCHANGE/NOCHANGE

\$GFNDC DCOP Z014G.04  
Entry constraint: DONTCARE/DONTCARE/DONTCARE/DONTCARE  
Exit constraint: NOCHANGE/NOCHANGE/NOCHANGE/NOCHANGE

\$GFODC DCOP Z004G.03  
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Exit constraint: NOCHANGE/NOCHANGE/NOCHANGE/NOCHANGE

\$GNTDC DCOP Z038G.02  
Entry constraint: DONTCARE/DONTCARE/DONTCARE/DONTCARE  
Exit constraint: NOCHANGE/NOCHANGE/NOCHANGE/NOCHANGE

\$GPLDC DCOP Z002G.03  
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Exit constraint: NOCHANGE/NOCHANGE/NOCHANGE/NOCHANGE

\$GTOX STRING DI-PANDA,D2-PANDA

\$LOTMPAN STRING F7,F5,D5-GUAVA

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Exit constraint: NOCHANGE/NOCHANGE/NOCHANGE/NOCHANGE

\$MTLDP1 STRING A11K

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\$NSDIMP STRING WC583-P31\_6.0E15@95KEV

\$PADE STRING PAD

\$PAVIMP STRING WZ250-B11\_2E15@35KEV

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\$PLYDP STRING 5K\_POLY

\$PLYPHOS STRING E4-TUNA

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\$PSDIMP STRING WI314-B11\_5.0E15@35KEV

\$R2 STRING WTCBS-R2A

\$R3 STRING WTCBS-R3A

\$R35 STRING WTCBS-R35A

\$R4 STRING WTCBS-R4A

\$R5 STRING WTCBS-R5A

\$R6 STRING WTCBS-R6A

\$R61 STRING WTCBS-R61A

\$R75 STRING WTCBS-R75A

\$R8 STRING WTCBS-R8A

\$REFLW STRING D4-BURMA/E2-VEST

\$SECAN STRING D5-LEMON/F5-LEMON

\$SILNITRDP STRING CPNT685A

\$STMox STRING F6-ASPEN

001.000 STARTING\_MATERIAL  
Location : DIFF

Stage: START




Document :  
 Desc. :  
 Traceable: Update Supply Trace Supply Update Dest.  
 Trace Dest.

	Part	Attribute
	001 WVEPIAA18	PRIMARY
002.000	CALL_PROCEDURE	<u>Stage:</u> DEFAULT
	Procedure: ZESCRBIP	
	Title : WAFER SCRIBE -- 105MM WAFERS	
003.000	CALL_PROCEDURE	<u>Stage:</u> DEFAULT
	Procedure: ZENIT5SG	
	Title : ACTIVE EXPOSE AND ETCH	
004.000	CALL_PROCEDURE	<u>Stage:</u> DEFAULT
	Procedure: ZEFLD5DM	
	Title : DMOS/ FIELD OX AND NTR REMOVAL	
005.000	CALL_PROCEDURE	<u>Stage:</u> DEFAULT
	Procedure: ZENRONDMS	
	Title : N+ IMPLANT/GATE OXIDATION MODULE DMOS	
006.000	CALL_PROCEDURE	<u>Stage:</u> DEFAULT
	Procedure: ZEPDP3SG	
	Title : 3u SAG W/POLY DEP/PHOS & IMPL.	
007.000	CALL_PROCEDURE	<u>Stage:</u> DEFAULT
	Procedure: ZEPLY5DMS	
	Title : POLY EXPOSE & ETCH DMOS	
008.000	CALL_PROCEDURE	<u>Stage:</u> DEFAULT
	Procedure: ZEPBDYIM	
	Title : P BODY & P+ AVALANCHE IMPLANT/DRIVE MODULE	
009.000	CALL_PROCEDURE	<u>Stage:</u> DEFAULT
	Procedure: ZEPSD5SG	
	Title : P+S/D EXPOSE AND IMPLANT	
010.000	CALL_PROCEDURE	<u>Stage:</u> DEFAULT
	Procedure: ZENS05SG	
	Title : N+S/D MASK AND IMPLANT 5u	
011.000	CALL_PROCEDURE	<u>Stage:</u> DEFAULT
	Procedure: ZEIDODMO	
	Title : INTERLAYER DOPED OXIDE/WITHOUT ARGON IMPLANT	
012.000	CALL_PROCEDURE	<u>Stage:</u> DEFAULT
	Procedure: ZECTN5SG	
	Title : CONTACT STEPPER & ETCH 5u (NO CRSI)	
013.000	CALL_PROCEDURE	<u>Stage:</u> DEFAULT
	Procedure: ZEBSCONTACT	
	Title : BACKSIDE CONTACT MODULE FOR HIGH POWER MOSFET	
014.000	CALL_PROCEDURE	<u>Stage:</u> DEFAULT
	Procedure: ZEMLODMS	
	Title : METAL DEP \$MTLDP1 LIFTOFF	
015.000	CALL_PROCEDURE	<u>Stage:</u> DEFAULT
	Procedure: ZEPADBIP	
	Title : PAD MODULE	
016.000	CALL_PROCEDURE	<u>Stage:</u> DEFAULT
	Procedure: ZEFANEAL	
	Title : FINAL ANNEAL MODULE 450 DEG	
017.000	CALL_PROCEDURE	<u>Stage:</u> DEFAULT
	Procedure: ZEKETHLY	

Title : KEITHLEY PROBE MODULE  
018.000 CALL\_PROCEDURE Stage: DEFAULT  
Procedure: ZEBGRALL  
Title : BACKGRIND MODULE - all processes  
019.000 CALL\_PROCEDURE Stage: DEFAULT  
Procedure: ZEBSMETAL  
Title : METAL DEP WAFER BACKSIDE (CALL ENG)  
020.000 CALL\_PROCEDURE Stage: DEFAULT  
Procedure: ZEFINVIS  
Title : Final Visual Inspection w/o pop.  
021.000 CALL\_PROCEDURE Stage: DEFAULT  
Procedure: ZETRNFER  
Title : WAFER TRANSFER  
022.000 MOVE\_TO\_LOCATION Stage: ENGINV  
Location : ENGINV



\*\*\*\*\*  
\*\*\*\*\*

Procedure : WTCBS-001A.04 PLANNABLE  
Title : 5 $\mu$  DMOS W/BSCONTACT HIGH POWER MOSFET 150MM  
Owner : FIX Date created :   
08:00  
Status : ACTIVE NOSTARTS Date last changed:   
16:29  
Access category: Date activated :   
09:48  
Procedure usage: PRIMARY\_PROCEDURE Main prod area : WAFERFAB  
ECN :  
Document : DEVICE WTCBS-001A.04

# Material constraints

Identity	Processing state	Main-Material type	Sub-Material
Entry: Nothing	Nothing	Nothing	Nothing
Exit : Identified	Normal	W = wafers	Nothing

No category has been specified.

No output part has been specified.

No material type conversions have been specified.

Parameter	Type	Value
\$BDIMP	STRING	WI660-B11_1.6E14@40KEV
\$BKGRND	STRING	19 MIL
\$CAPOX	STRING	D8-ORCID
\$D	STRING	WTCBS-001A
\$DCODC	DCOP	Z129D.02
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	Exit constraint:	NOCHANGE/NOCHANGE/NOCHANGE/NOCHANGE
\$DFODC	DCOP	Z087D.01
	Entry constraint:	DONTCARE/DONTCARE/DONTCARE/DONTCARE
	Exit constraint:	NOCHANGE/NOCHANGE/NOCHANGE/NOCHANGE
\$DGTDC	DCOP	Z147D.01
	Entry constraint:	DONTCARE/DONTCARE/DONTCARE/DONTCARE
	Exit constraint:	NOCHANGE/NOCHANGE/NOCHANGE/NOCHANGE
\$DPOX	STRING	7K_7_PSG
\$DRFDC	DCOP	Z090D.01
	Entry constraint:	DONTCARE/DONTCARE/DONTCARE/DONTCARE
	Exit constraint:	NOCHANGE/NOCHANGE/NOCHANGE/NOCHANGE
\$DSTDC	DCOP	Z088D.01
	Entry constraint:	DONTCARE/DONTCARE/DONTCARE/DONTCARE
	Exit constraint:	NOCHANGE/NOCHANGE/NOCHANGE/NOCHANGE
\$ECTDC	STRING	NO_DATA_NEEDED
\$ENTDC	DCOP	Z060E.01
	Entry constraint:	DONTCARE/DONTCARE/wafers/DONTCARE
	Exit constraint:	NOCHANGE/NOCHANGE/wafers/NOCHANGE
\$FLDOX	STRING	D7-WHITE,F3-WHITE
\$FNLPAS	STRING	4K0X_4KNIT